

Search Results -

Terms	Documents
14 same different width	1

US	Patents Full-Text Database	_
	O Abstracts Database	
EP	O Abstracts Database	
De	rwent World Patents Index	
I IRN	Technical Disclosure Bulletins	Ξ

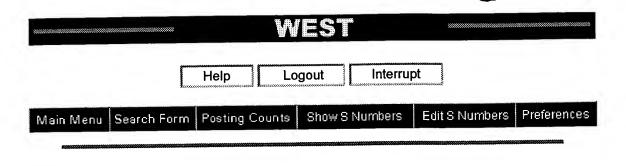
42-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1

Refine Search: Clear

Search History

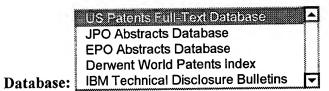
Today's Date: 8/8/2000

DB Name	<u>Query</u>	Hit Count	Set Name
USPT	14 same different width	1	<u>L8</u>
USPT	14 near5 width	11	<u>L7</u>
USPT	14 same (concatenat\$4 or catenat\$3)	1	<u>L6</u>
USPT	14 and condec	0	<u>L5</u>
USPT	(multiple or plurality or more than one or numerous) near3 data path	576	<u>L4</u>
USPT	5600814.uref.	1	<u>L3</u>
USPT	5600814.uref.	1	<u>L2</u>
USPT	5594877.uref.	4	<u>L1</u>



Search Results -

Terms	Documents
12 and different width	2

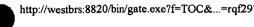


	12 and	different	width		
Refine Search:	***************************************			₹	Clear

Search History

Today's Date: 8/8/2000

DB Name	<u>Query</u>	Hit Count	Set Name
USPT	12 and different width	2	<u>L12</u>
USPT	12 same (different or multiple or plurality) near4 width	3	<u>L11</u>
USPT	12 near3 copy\$3	8	<u>L10</u>
USPT	12 and 13	4	<u>L9</u>
USPT	13 and 14	1	<u>L8</u>
USPT	11 and 12	0	<u>L7</u>
USPT	11 same 12	0	<u>L6</u>
USPT	13 same 14	1	<u>L5</u>
USPT	low order same 32 bit near8 64 bit	44	<u>L4</u>
USPT	high order same 16 bit near8 32 bit	96	<u>L3</u>
USPT	first memory near3 portion	702	<u>L2</u>
USPT	(plurality or multiple) near3 data path near8 width	11	<u>L1</u>



Generate Collection

Search Results - Record(s) 1 through 24 of 24 returned.

☐ 1. Document ID: US 6047348 A

L1: Entry 1 of 24

File: USPT

Apr 4, 2000

DOCUMENT-IDENTIFIER: US 6047348 A

TITLE: System and method for supporting a multiple width memory

subsystem

URPN: 5280598

Full Title Citation Front Review Classification Date Reference Claims KMC Draw. Desc Image

2. Document ID: US 6006303 A

L1: Entry 2 of 24

File: USPT

Dec 21, 1999

DOCUMENT-IDENTIFIER: US 6006303 A

TITLE: Priority encoding and decoding for memory architecture

URPN: 5280598

Full Title Citation Front Review Classification Date Reference Claims KWIC Draw Desc Image

3. Document ID: US 5960453 A

L1: Entry 3 of 24

File: USPT

Sep 28, 1999

DOCUMENT-IDENTIFIER: US 5960453 A

TITLE: Word selection logic to implement an 80 or 96-bit cache

SRAM

URPN: 5280598

Full Title Citation Front Review Classification Date Reference Claims KWIC Draw Desc Image

L1: Entry 4 of 24

File: USPT

Mar 23, 1999

DOCUMENT-IDENTIFIER: US 5887148 A

4. Document ID: US 5887148 A

TITLE: System for supporting a buffer memory wherein data is stored in multiple data widths based upon a switch interface

for detecting the different bus sizes

URPN: 5280598

Full Title Citation Front Review Classification Date Reference Claims KMC Draw Desc Image

5. Document ID: US 5870573 A

L1: Entry 5 of 24

File: USPT

Feb 9, 1999

DOCUMENT-IDENTIFIER: US 5870573 A

TITLE: Transistor switch used to isolate bus devices and/or

translate bus voltage levels

URPN: 5280598

Full | Title: | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image |

6. Document ID: US 5867672 A

L1: Entry 6 of 24

File: USPT

Feb 2, 1999

DOCUMENT-IDENTIFIER: US 5867672 A

TITLE: Triple-bus FIFO buffers that can be chained together to

increase buffer depth

URPN: 5280598

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image |

7. Document ID: US RE36052 E

DOCUMENT-IDENTIFIER: US RE36052 E

TITLE: Data processor with bus-sizing function

URPN: 5280598

Full Title Citation Front Review Classification Date Reference Claims KWIC Draw Desc Image

8. Document ID: US 5835960 A

L1: Entry 8 of 24

L1: Entry 7 of 24

File: USPT

File: USPT

Nov 10, 1998

Jan 19, 1999

DOCUMENT-IDENTIFIER: US 5835960 A

TITLE: Apparatus and method for interfacing a peripheral device

having a ROM BIOS to a PCI bus

URPN: 5280598

Full Title Citation Front Review Classification Date Reference Claims KWC Draw Desc Image

9. Document ID: US 5768546 A

L1: Entry 9 of 24

File: USPT

Jun 16, 1998

DOCUMENT-IDENTIFIER: US 5768546 A

TITLE: Method and apparatus for bi-directional transfer of data

between two buses with different widths

URPN: 5280598

Full Title Citation Front Review Classification Date Reference Claims KMC Draw Desc Image

10. Document ID: US 5768608 A

L1: Entry 10 of 24

File: USPT

Jun 16, 1998

TITLE: Data processing apparatus and method for making same

URPN: 5280598

Full Title Citation Front Review Classification Date Reference Claims KMC Draw Desc Image

11. Document ID: US 5748919 A

DOCUMENT-IDENTIFIER: US 5768608 A

L1: Entry 11 of 24

File: USPT

May 5, 1998

DOCUMENT-IDENTIFIER: US 5748919 A

TITLE: Shared bus non-sequential data ordering method and

apparatus

URPN: 5280598

Full Title Citation Front Review Classification Date Reference Claims KWC Draw Desc Image

12. Document ID: US 5724604 A

L1: Entry 12 of 24

File: USPT

Mar 3, 1998

DOCUMENT-IDENTIFIER: US 5724604 A

TITLE: Data processing system for accessing an external device

and method therefor

URPN: 5280598

Full Title Citation Front Review Classification Date Reference Claims KWC Draw Desc Image

13. Document ID: US 5671373 A

L1: Entry 13 of 24

File: USPT

Sep 23, 1997

http://westbrs:8820/bin/gate.exe?f=TOC&...=rqf297.22cef=1&dbname=USPT&ESNAME=KWIC

DOCUMENT-IDENTIFIER: US 5671373 A

TITLE: Data bus protocol for computer graphics system

URPN: 5280598

Full Title Citation Front Review Classification Date Reference Claims KWC Draw Desc Image

14. Document ID: US 5630099 A

L1: Entry 14 of 24

File: USPT

May 13, 1997

DOCUMENT-IDENTIFIER: US 5630099 A

TITLE: Non-volatile memory array controller capable of controlling memory banks having variable bit widths

URPN: 5280598

Full Title Citation Front Review Classification Date Reference Claims KMC Draw Desc Image

15. Document ID: US 5613078 A

L1: Entry 15 of 24

File: USPT

Mar 18, 1997

DOCUMENT-IDENTIFIER: US 5613078 A

TITLE: Microprocessor and microprocessor system with changeable

effective bus width

URPN: 5280598

Full Title Citation Front Review Classification Date Reference Claims KWIC Draw Desc Image

16. Document ID: US 5600814 A

L1: Entry 16 of 24

File: USPT

Feb 4, 1997

DOCUMENT-IDENTIFIER: US 5600814 A

TITLE: Data processing unit for transferring data between

devices supporting different word length

URPN: 5280598

Full Title Citation Front Review Classification Date Reference Claims KWIC Draw Desc Image

17. Document ID: US 5594877 A

L1: Entry 17 of 24

File: USPT

Jan 14, 1997

DOCUMENT-IDENTIFIER: US 5594877 A

TITLE: System for transferring data onto buses having different

widths

URPN: 5280598

Full Title Citation Front Review Classification Date Reference Claims KMC Draw Desc Image

18. Document ID: US 5590378 A

L1: Entry 18 of 24

File: USPT Dec 31, 1996

DOCUMENT-IDENTIFIER: US 5590378 A

TITLE: Apparatus for aligning and padding data on transfers between devices of different data widths and organizations

URPN: 5280598

Full Title Citation Front Review Classification Date Reference Claims KWIC Draw Desc Image

19. Document ID: US 5579530 A

L1: Entry 19 of 24

File: USPT

Nov 26, 1996

http://westbrs:8820/bin/gate.

DOCUMENT-IDENTIFIER: US 5579530 A TITLE: Method and apparatus for dynamically allocating access time to a resource shared between a peripheral bus and a host bus by dynamically controlling the size of burst data transfers on the peripheral bus

URPN: 5280598

Full Title Citation Front Review Classification Date Reference Claims KWIC Draw Desc Image

20. Document ID: US 5553244 A

L1: Entry 20 of 24

File: USPT

Sep 3, 1996

DOCUMENT-IDENTIFIER: US 5553244 A

TITLE: Reflexively sizing memory bus interface

URPN: 5280598

Full Title Citation Front Review Classification Date Reference Claims KWC Draw. Desc Image

21. Document ID: US 5553252 A

L1: Entry 21 of 24

File: USPT

Sep 3, 1996

DOCUMENT-IDENTIFIER: US 5553252 A

TITLE: Device for controlling data transfer between chips via a

bus

URPN: 5280598

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

22. Document ID: US 5440708 A

L1: Entry 22 of 24

File: USPT

Aug 8, 1995

DOCUMENT-IDENTIFIER: US 5440708 A

TITLE: Microprocessor and storage management system having said

microprocessor

URPN: 5280598

Full Title Citation Front Review Classification Date Reference Claims KWC Draw. Desc Image

23. Document ID: US 5396597 A

L1: Entry 23 of 24

File: USPT

Mar 7, 1995

DOCUMENT-IDENTIFIER: US 5396597 A

TITLE: System for transferring data between processors via dual buffers within system memory with first and second processors

accessing system memory directly and indirectly

URPN: 5280598

Full Title Citation Front Review Classification Date Reference Claims KWC Draw Desc Image

24. Document ID: US 5394528 A

L1: Entry 24 of 24

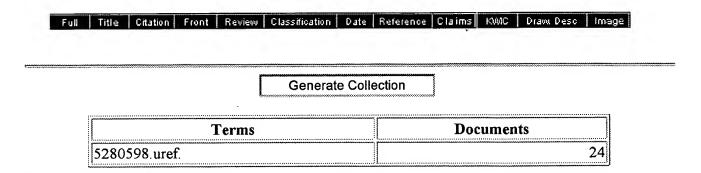
File: USPT

Feb 28, 1995

DOCUMENT-IDENTIFIER: US 5394528 A

TITLE: Data processor with bus-sizing function

URPN: 5280598



Display

50 Documents, starting with Document: 24

Display Format: KWIC

Change Format